CLAIMS

Having thus described our invention in detail, what we claim as new and desire to secure by the Letters Patent is:

1. A bipolar transistor comprising:

an emitter comprising an intrinsic emitter portion and an extrinsic emitter portion;

a base comprising an intrinsic base portion in electrical contact with said intrinsic emitter portion and an extrinsic base portion in electrical contact with said intrinsic base portion and electrically isolated from said extrinsic emitter portion by emitter/base spacers, wherein said extrinsic emitter portion is recessed below an upper surface of said extrinsic base portion; and

a collector in electrical contact with said intrinsic base portion.

2. The bipolar transistor of Claim 1 wherein said extrinsic base portion comprises an upper surface that is silicided to said emitter/base spacers.

3. The bipolar transistor of Claim 1 wherein said collector further comprises a vertically narrow pedestal dopant region.

4. The bipolar transistor of Claim 1 wherein each emitter/base spacer of said emitter/base spacers have a width ranging from about 22.5 nm to about 27.5 nm.

5. A bipolar transistor comprising:

an emitter;

a base comprising an intrinsic base portion in electrical contact with said emitter and an extrinsic base portion in electrical contact with said intrinsic base portion and electrically isolated from said emitter by emitter/base spacers, wherein an upper surface of said extrinsic base portion is silicided to said emitter/base spacers; and

a collector in electrical contact with said intrinsic base portion.

6. The bipolar transistor of Claim 5 wherein said emitter is recessed beneath said upper surface of said extrinsic base portion.

7. A bipolar transistor comprising:

an emitter;

a base comprising an intrinsic base portion in electrical contact with said emitter and an extrinsic base portion in electrical contact with said intrinsic base portion and electrically isolated from said emitter;

a collector comprising an intrinsic collector portion surrounded by an extrinsic collector, said intrinsic collector portion in electrical contact with said intrinsic base portion, wherein an active area of said bipolar transistor includes at least said intrinsic collector portion and said intrinsic base portion; and

a base window dielectric positioned between said extrinsic collector and said extrinsic base portion, wherein said base window dielectric extends into said active area of said bipolar transistor.

8. The bipolar transistor of Claim 7 wherein said emitter is recessed beneath an upper surface of said extrinsic base portion.

9. The bipolar transistor of Claim 7 wherein silicide regions cover substantially entire surface of said extrinsic base portion.

10. The bipolar transistor of Claim 7 wherein said collector further comprises a narrow pedestal implant region, wherein said narrow pedestal implant region has a peak dopant concentration abutting said extrinsic collector.

11. A method of forming a bipolar transistor comprising the steps of:

forming a collector;

forming an intrinsic base above said collector;

forming extrinsic base regions separated by an emitter channel, said emitter channel exposing an upper surface of said intrinsic base;

forming emitter/base spacers on vertical surfaces of each of said extrinsic base regions;

forming an emitter within said emitter channel, wherein said emitter is recessed below an upper surface of said extrinsic base regions;

forming an isolation stack atop at least said extrinsic base regions and said emitter;

forming a dielectric layer atop said isolation stack;

providing an emitter via through said dielectric layer and said isolation stack to expose said emitter and a portion of said extrinsic base regions; and

forming contact isolation spacers within said emitter via to provide electrical isolation between said recessed emitter and said extrinsic base regions, wherein a portion of said recessed emitter remains exposed.

12. The method of Claim 11 further comprising providing electrical connectivity to said emitter, said extrinsic base regions and said collector.

13. The method of Claim 11 wherein said forming said emitter within said emitter channel comprises depositing:

a layer of polysilicon atop at least said emitter channel;

planarizing said layer of polysilicon coplanar with horizontal surfaces of said extrinsic base regions; and

recessing said layer of polysilicon by selective etching.

14. The method of Claim 11 wherein an upper surface of said emitter and horizontal surfaces of said extrinsic base regions are silicided, wherein said silicide regions extend to said emitter/base spacers.

15. The method of Claim 11 wherein said collector further comprises a pedestal dopant region, said pedestal dopant region is formed by implanting an n-type dopant at a concentration ranging from $2x10^{11}$ atoms/cm^2 to about $1x10^{13}$ atoms/cm^2 at an energy ranging from about 30 keV to about 50 keV.

16. A method of forming a bipolar transistor comprising the steps of:

forming a collector;

forming an intrinsic base above said collector;

forming extrinsic base regions separated by an emitter channel, said emitter channel exposing an upper surface of said intrinsic base;

forming emitter/base spacers on vertical surfaces of said extrinsic base regions;

forming an emitter within said emitter channel;

forming silicide contacts on at least said extrinsic base and said emitter, wherein a top surface of said extrinsic base is silicided to said emitter/base spacers;

forming a isolation stack atop at least said extrinsic base regions and said emitter;

forming a dielectric layer atop said isolation stack;

providing an via through said dielectric layer and said isolation stack to expose said emitter and a portion of said extrinsic base regions; and

forming contact isolation spacers within said via to provide electrical isolation between said emitter and said extrinsic base regions, wherein a portion off said emitter remains exposed.

17. A method of forming a bipolar transistor comprising the steps of:

forming a first conductivity epitaxially grown silicon-containing layer atop second conductivity portion of a substrate;

forming at least two isolation regions in said first conductivity epitaxially grown silicon-containing layer, wherein an active area is formed between said at least two isolation regions;

forming a base window dielectric layer atop said first conductivity epitaxially grown silicon-containing layer and said at least two isolation regions; wherein said base window dielectric within said active area;

forming first conductivity extrinsic base regions, each first conductivity epitaxial base region of said first conductivity extrinsic base regions separated by an emitter channel, said emitter channel exposing a portion of said first conductivity epitaxially grown silicon-containing layer; and

forming a second conductivity emitter within said emitter channel, wherein said emitter is separated from said first conductivity extrinsic base regions by emitter/base spacers.

18. The method of Claim 17 wherein said first conductivity epitaxially grown silicon-containing layer has a thickness less than about 0.6 μm.

19. The method of Claim 17 wherein said emitter is recessed below a horizontal surface of said set of first conductivity extrinsic base regions.

20. The method of Claim 17 wherein said horizontal surface of said set of first conductivity extrinsic base regions is silicided to said emitter/base isolation spacer.